SIMULATION OF ANALOG FLANGER EFFECT USING BBD CIRCUIT

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ABSTRACT

This paper deals with simulation of BBD circuit based analog flanger effects. The famous Electro-Harmonix Deluxe Electric Mistress flanger effect was used as a case study in this paper. The main attention of this paper is paid to the analysis and simulation of the LFO circuit, the BBD clock generator circuit and BBD circuit simulation of this effect. However, in order to compare the simulation results with measured data, the signal path simulation using the DK-method has been introduced as well.

1. INTRODUCTION

A delay line is an essential part of many audio effects, foremost delay effects and some modulation effects like chorus and flanger. The construction of these audio effects has been known since late 1960s when the bucket-brigade device (BBD) was invented by F. Sangster in Philips Research Labs [1, 2]. The BBD is basically an analog shift register to shift the electrical charge, representing the input signal, along internal capacitors. The resulting delay time is given by the number of the internal capacitors and by the period of the clock signal which is used to control the shifting the charge inside the BBD. The clock signal could be modulated by a low frequency oscillator (LFO) in order to obtain a time-variable delay typical for chorus and flanger audio effects. Although the BBD has been still used especially for analog guitar effect pedals, digital implementations of modulation effects became more popular. The delay line is realized by a circular buffer in the memory where the time delay is given by the length of the circular buffer. Because the simple circular buffer provides only a discrete time delays equal to an integer multiple of the sampling period, fractional delay lines have been introduced for audio effects which require any value of delay time to work properly – e.g. modulation effects where the delay time is modulated by the digital LFO [3]. The fractional delay line is implemented using the circular buffer and the neighboring samples in the circular buffer are interpolated in order to obtain the time delay of any value. Linear interpolation, spline interpolation or finite impulse response (FIR) filter are often used as interpolators with different sonic qualities and computational demands [3]. The latest generation of the digital audio effects however tents to emulate sonic qualities of their analog models by simulation of their electric circuits in real time. Many types of such audio effects were simulated during last years, foremost guitar amplifiers with tubes, guitar distortion pedals, guitar compressor pedals, guitar wah pedals, etc. The audio delay effects with the BBD are the main topic in paper [4]. The general structure of such effects is described and further, simulation of some parts of these effects is introduced there – namely antialiasing and reconstruction filters and compandor circuit used in analog delay guitar pedals. The BBD circuit is simulated using the black box approach – by measurement of frequency response and harmonic distortion and their simulation using a simple digital filter and waveshaping technique alt-hough an approach for the BBD circuit has been proposed. Because the authors dealt foremost with delay audio effect analysis and simulation where the delay time is fixed and the clock signal generation unit has not been described there, foremost the simulation of the clock generation circuit and a simple model of the BBD circuit are described in this paper.

2. CIRCUIT ANALYSIS AND SIMULATION

The Electro-Harmonix Deluxe Electric Mistress effect has been used as case study in this paper. Although it is possible to perform the simulation of the whole circuit, this approach is not suitable for real time simulation due to high computational demands and therefore a division into separate functional units is used.

2.1. Low frequency oscillator

The low frequency oscillator circuit very often comprises of an integrator and a comparator circuits connected in a feedback loop. The circuit schematic of the LFO is shown in Figure 1. The simulation of this circuit using the DK method is fully described in [6]. This circuit generates a triangle signal with the frequency given by R_1, R_2, R_3 and C_1 values. The R_1 resistor is often a potentiometer to control the LFO speed.
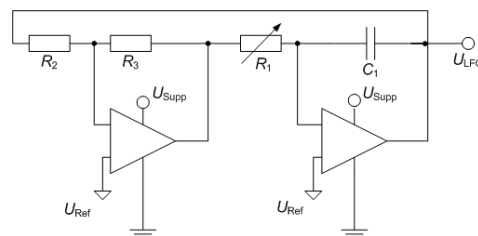

Figure 1: *Typical LFO circuit.*

The first operational amplifier (OPA) is the non-inverting comparator with hysteresis

$$U_\mathrm{H} = 2U_\mathrm{Supp} \frac{R_2}{R_3} \qquad (1)$$

and the second OPA serves as the integrator with the output

$$U_\mathrm{LFO}(t) = U_\mathrm{Ref} - \frac{1}{R_1 C_1} \int \pm\left(U_\mathrm{Supp} - U_\mathrm{Ref}\right) dt, \qquad (2)$$

giving, together with the comparator, the integration time

$$t_\mathrm{Int} = 2 \frac{R_1 R_2 C_1}{R_3} \qquad (3)$$

and LFO frequency $f = \frac{1}{2t_\mathrm{Int}}$. U_Supp is the OPA power supply and U_Ref is the virtual zero voltage offset.

The digital simulation of this circuit might be implemented according to

$$U_\mathrm{LFO}[n+1] = U_\mathrm{LFO}[n] + s \frac{U_\mathrm{Supp}}{R_1 C_1 T_\mathrm{s}}, \qquad (4)$$

where T_s is the sampling period, boundary condition $U_{\text{LFO}}[0] = U_{\text{Ref}}$ and $s = \pm 1$. The sign s is changed to the opposite value every time when the LFO output signal exceeds the comparator thresholds

$$U_{\text{LFO}}[n+1] > U_{Ref} + \left(U_{\text{Supp}} - U_{\text{Ref}}\right)\frac{R_2}{R_3} \qquad (5)$$

or

$$U_{\text{LFO}}[n+1] < U_{Ref} - \left(U_{\text{Supp}} - U_{\text{Ref}}\right)\frac{R_2}{R_3}. \qquad (6)$$

2.2. Clock generation unit

The BBD chip cannot operate only by itself and requires clock signals to control the BBD chip provided by the clock generation unit. In contrast to the LFO circuit, this circuit is often unique for audio effect manufacturers and for specific audio effects. However some general characteristic can be found as well. A triangle signal from the LFO is typically filtered by a low pass filter to shape the LFO signal to a sine wave by filtering higher harmonics. The filtered LFO signal is used to control an astable oscillator generating the clock signal. It could be either an integrated circuit (e.g. MN3101 with an internal or an external oscillator) or it is also possible to generate the clock signal using discrete circuit parts – an astable circuit and a flip-flop chip generating two phase opposite signals as can be seen in Figure 2 which shows the clock generation unit of the Electro-Harmonix Deluxe Electric Mistress effect [5].
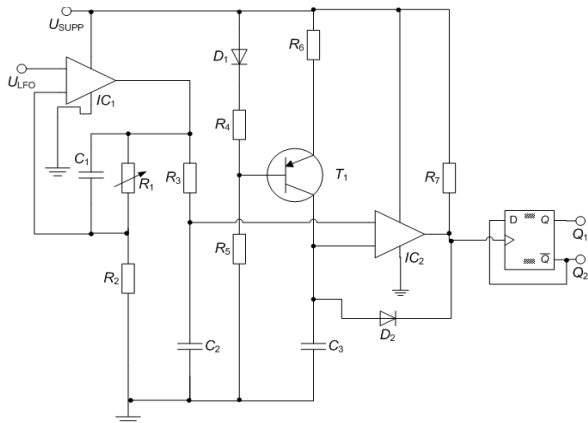

Figure 2: *Clock generator circuit of Electro-Harmonix Deluxe Electric Mistress effect.*

The input low pass filter consists of OPA IC_1, potentiometer R_1, resistors R_2, R_3 and capacitors C_1 and C_2. The transfer function of the low pass filter is given by

$$H(p) = \frac{C_1 R_1 p + 1}{C_1 C_2 R_1 R_3 p^2 + (C_2 R_3 + C_1 R_1)p + 1} \qquad (7)$$

and a corresponding digital filter can be designed using the bilinear transform of the transfer function (7).

The second part of the circuit is the clock generator. The main principle is based on charging and discharging of the capacitor C_3. The capacitor is charged via collector current from the transistor T_1 until the capacitor voltage is equal to threshold voltage from the low pass filter, then the comparator IC_2 is switched to low output value and the capacitor C_3 is immediately discharged via the high speed diode D_2 and the comparator output switches back to the original high output value. The whole process is being repeated as can be seen from Figure 3. Simulation of the circuit could be solved in real time like other audio circuit using an appropriate method (e.g. DK-method) but duration of transients is shorter than a typical sampling period and therefore the simu-

lation would have to run at very high sampling frequencies. The most important information is not however the signal itself but rather the time when the signal reaches the threshold value. Supposing an approximation of the step response of the simulated circuit with a step response of a passive RC network given by

$$U_{\text{THD}} = U_{\text{Max}}\left(1 - e^{-\frac{t}{\tau}}\right), \qquad (8)$$

with approximation parameters τ (equal to the time constant), U_{Max} (equal to the max voltage which can be reached) and U_{THD} (the voltage to which the capacitor should be charged), the unknown time t can be expressed using

$$t = -\tau \log\left(\frac{U_{\text{Max}} - U_{\text{THD}}}{U_{\text{Max}}}\right), \qquad (9)$$

on the condition that the U_{THD} voltage is constant or is being changed very slowly during the integration. For slowly changing voltage U_{THD}, a linear interpolation can be used to formulate the equation

$$\frac{U_{\text{THD}}(t_0+t) - U_{\text{THD}}(t_0)}{t} = U_{\text{Max}}\left(1 - e^{-\frac{t}{\tau}}\right), \qquad (10)$$

where t_0 is the boundary condition and t the unknown integration time. Because the time t cannot be simply isolated from equation (10), a numerical method must be used to get the integration time.
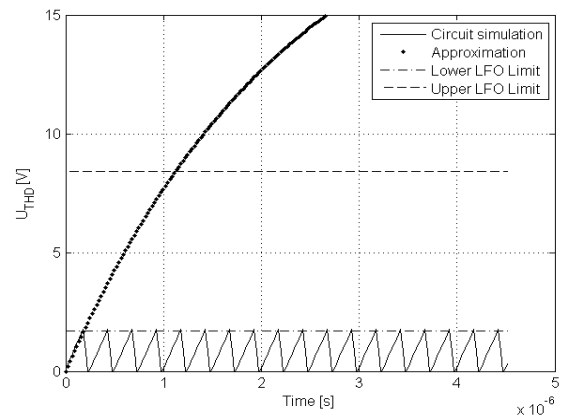

Figure 3: *Step response of the astable circuit and its approximation.*

The astable oscillator output signal is connected to the clock input of the flip-flop chip which reacts on the rising edge, the data port of the flip flop chip is connected to the output port Q_2 in order to flip the output to the opposite state, generating two opposite clock signals for the BBD with the period equal to

$$T_{\text{Clock}} = 2t \qquad (11)$$

at Q_1 and Q_2 output ports.

2.3. BBD simulation

There have been used more types of BBD chips from different manufactures (e.g. MNxxx chips made by Panasonic and SADxxx manufactured by Reticon company) in guitar effects. Basically, the internal structure is very similar, consisting of a series of MOS transistors used as switches and capacitors used to hold the electric charge. The simplified circuit topology is shown in Figure 4 [4]. The first transistor and capacitor are used for sampling of an input signal. The rest of the circuit consist of charge holding elements which are separated by DC biased gates enhancing the charge transfer [2]. The neighboring charge holding elements are controlled using two anti-phase clock signals in such way that neighboring switches are in opposite states in order to pass the electric charge only into a subsequent stage.
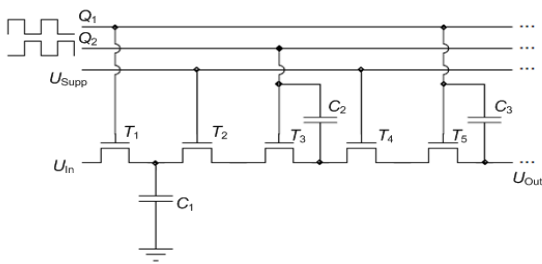
Figure 4: *Simplified BBD circuit topology.*

The crucial difference between the BBD delay line and the variable circular buffer used for implementation of a delay line in digital effects is that the BBD has a fixed number of cells. In case of variable circular buffer, the desired delay is obtained using variable number of delay cells but the input and output signal samples are written and read with a constant sampling period. On the contrary, a variable sampling period is required to obtain the desired delay from the BBD delay line. It means that for the digital implementation of the BBD delay line we have to match the digital effect sampling period with the BBD sampling period. An oversampling can be used to match the sampling periods for static delay times, as has already been suggested in [4]. However, more challenging is when the BBD sampling period is modulated by the LFO. In this case, there is no constant relation to match the sampling periods and an interpolation of the input and output signals is required because the BBD sampling can occur at any time between the input and output signal samples. An algorithm based on this principle has been designed and its flowchart describing processing of one signal sample is shown in Figure 5. The algorithm uses one variable tTemp to store the time increments. This variable is initialized to the BBD clock period obtained from (9).While it is greater than a sampling period T_s, it is decremented by T_s and output signal samples are read from the BBD. If the tTemp is less than T_s, the new input sample for the BBD is acquired, signal samples stored in the BBD delay line are shifted and new clock period is computed from (9) and added to tTemp. Because the BBD sampling occurs between audio signal samples, linear interpolation is used, as shown in Figure 5. The samples in the delay cells are shifted according to $bbd[2n + m + 1] = bbd[2n + m]$ for $n \in \langle 0, \frac{N}{2} - 1 \rangle$ and $m = modulo_2(m + 1)$ where N is number of cells of the BBD chip (512 for SAD1024 BBD used in this effect) and bbd is the delay line to store the samples.

The model might be further extended with integrated filters simulating frequency dependent electric charge transfer between the cells. The filtration can be done e.g. using $bbd[2n + m + 1] += \frac{T_{Clock}}{\tau}(bbd[2n + m] - bbd[2n + m + 1])$ with T_{Clock} given by (9) and τ is filter time constant. Ideally, each cell transfer should be further process by a nonlinear function to simulate the transistors nonlinearities.
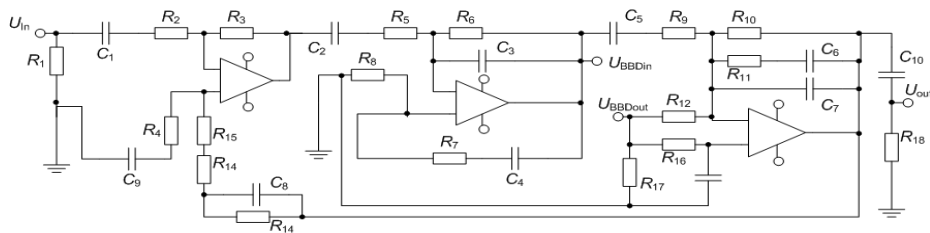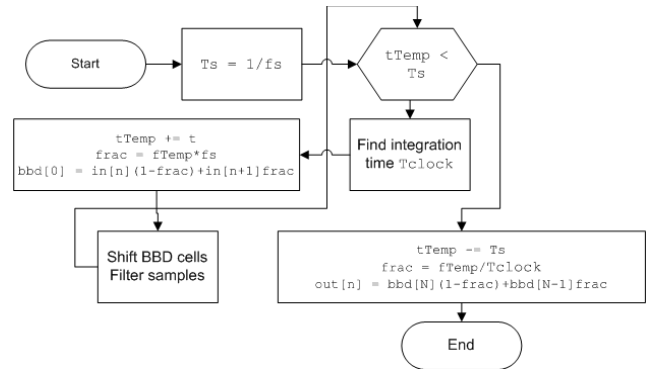

Figure 5: *BBD chip simulation algorithm –processing for one audio sample.*

Both nonlinear processing and filtration for each cell transfer however introduce very high computational demands when real-time processing is considered and both can be replaced by the BBD output sample filtering and nonlinear processing with characteristic e.g. according to paper [4].

2.4. Main signal path

Figure 6 shows the direct signal path consisting of the summation amplifier, antialiasing and reconstruction filters and SAD1024 BBD. The BBD line is connected to the nodes U_{BBDin} and U_{BBDout}. The whole signal path circuit except the BBD circuit can be simulated using different approaches. However, the challenge is the instantaneous feedback causing the flanger effect. The approach using the division of the signal path circuit into subcircuits would require adding a unit delay into the global feedback loop changing the overall frequency response of the circuit, as it was already shown in [6] where the unit delay was used in the tube guitar power amplifier simulation. Therefore simulation of the whole signal path circuit as one block is used. The nodal DK method with incidence matrices defined in [7] is a suitable method. Because the circuit contains operational amplifiers, an extension of the DK method introduced in [6] is used. The whole circuit can be described by the conductance matrix

$$S = \begin{pmatrix} N_R^T G_R N_R + N_X^T G_X N_X & N_u^T & N_{OPA-O}^T \\ N_u & 0 & 0 \\ N_{OPA-O} + A N_{OPA-I} & 0 & 0 \end{pmatrix} \quad (12)$$

where N_R, N_X, N_u, are incidence matrices, G_R and G_X resistors and capacitors conductance matrices all defined in [7] and N_{OPA-I}, N_{OPA-O} are incidence matrices and A is the vector of OPAs amplifications all defined in [6]. A linear model of the OPA given by $U_{Out} = A(U^+ - U^-)$ is used. Except the linearized OPAs, there are no other nonlinear circuit elements and thus the circuit can be described by a linear state space representation given by

Figure 6: *Circuit schematic of the signal path of the flanger effect.*

$$\boldsymbol{X} = \boldsymbol{AX} + \boldsymbol{BU}$$
$$\boldsymbol{Y} = \boldsymbol{DX} + \boldsymbol{EU} \tag{13}$$

where inputs vector is given by $\boldsymbol{U} = \begin{bmatrix} U_{\text{In}}[n] \\ U_{\text{BBDout}}[n] \end{bmatrix}$, outputs vec-

tor is given by $\boldsymbol{Y} = \begin{bmatrix} U_{out}[n] \\ U_{\text{BBDin}}[n] \end{bmatrix}$, matrices $\boldsymbol{A}$, $\boldsymbol{B}$, $\boldsymbol{D}$ and $\boldsymbol{E}$ are lin-

ear system state space matrices derived according to [7] from the conductance matrix $\boldsymbol{S}$ defined in (12), vector $\boldsymbol{X}$ is the system state vector and n is the sampling period index. The secondary input $U_{\text{BBDout}}[n]$ and output $U_{\text{BBDin}}[n]$ are connected to the BBD delay line implemented using the algorithm from Figure 5.

3. SIMULATION RESULTS

In order to prove the validity of the proposed algorithm, the algorithm was implemented in Matlab and the frequency response of the real flanger effect was measured. Because it is the time variable effect, it is generally difficult to evaluate the simulation only by measurement and comparison of the frequency responses of measured and simulated effect. However this flanger effect has a switch (called filter matrix on the effect box) bypassing the LFO circuit. In this regime, the input low pass filter in the clock generation circuit is fed up with constant voltage 1.7 V, this input voltage is amplified by the low pass filter using potentiometer R_1 in IC_1 feedback yielding the comparator threshold voltages within $U_{\text{THD}} \in (1.7, 8.4)$ V for all settings of the potentiometer R_1 (called „*Range*") in Figure 3. This static regime allows to measure the frequency response of the effect. Figures 7 and 8 show comparison of the measured and simulated frequency responses. The sampling frequency used for the simulation was equal to 96 kHz to match the frequency responses at higher frequencies otherwise warped by the bilinear transform. The length of the BBD was 512 samples and the integration time was adjusted by resistor R_6 in Figure 3, which has the same function (with wide range of settings) in the original circuit, to match the frequency responses.

Additionally, the algorithm was implemented in C++ language as a VST plugin and was able to run in real-time. The implementation of the BBD line requires shifting and filtering of all stored samples few times during one sampling period which is computationally very demanding for simulation in real time. To decrease the computational demands, the BBD line can by implemented as a fixed delay line using a circular buffer instead of shifting all the delay cells and further the low pass filtering between the delay cells can be omitted. This however can affect the effect frequency responses of the effect at high frequencies.

4. CONCLUSIONS

Simulation of the Electro-Harmonix Deluxe Electric Mistress flanger effect was described in this paper. The main attention was paid to simulation of the clock signal generation circuit and the BBD circuit. In contrast to the standard digital delay line implementations, the BBD delay line consist of fixed number of delay cells and the variable delay is obtained using different speed of reading the data from the delay line. The main signal path of the flanger effect was simulated using the nodal DK-method with incidence matrices. The novelty is use of the incidence matrices for operational amplifiers allowing simulation of the whole signal path circuit including the global feedback without dividing the circuit into blocks. The results showed good match between the simulated and measured frequency responses of the flanger effect proving validity of the proposed simulation algorithm.
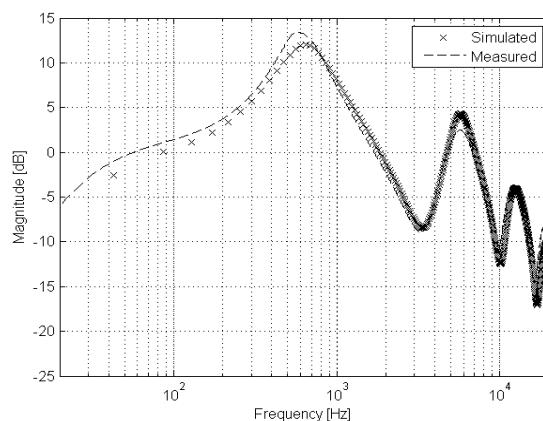
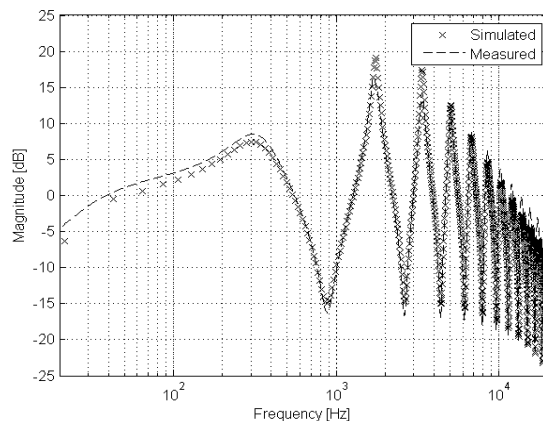Figure 7: *Frequency responses for min range parameter.*

Figure 8: *Frequency responses for max range parameter.*

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